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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,965	11/26/2003	Fujio Takeda	SIG000116	9518

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EXAMINER	
DANG, ROBERT TRONG	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,965	TAKEDA, FUJIO	
	Examiner	Art Unit	
	Robert T. Dang	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *5-8 and 13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-4, and 11-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Takeda (6385021). Takeda discloses in figure 1, an electrostatic discharge (ESD) protection circuit for an integrated circuit, the ESD protection circuit comprises: ESD clamping circuit (4) made up of elements operably coupled to a first power pin (1) of the integrated circuit and a second power pin (2) of the integrated circuit; ESD triggering circuit (8) operably coupled to the ESD clamping circuit, wherein, when enabled and when sensing an ESD event, the ESD triggering circuit provides a clamping signal to the ESD clamping circuit such that the ESD clamping circuit provides a low impedance path between the first and second power pins; and ESD disabling circuit operably coupled to disable the ESD triggering circuit when the integrated circuit is in a normal operating mode (see col. 1, lines 40-65)

As to claim 2, Takeda discloses in figure 1 element 4, wherein the ESD clamping circuit comprises at least one of: a **transistor**, a surge suppressor, and a silicon controlled rectifier.

As to claims 4 and 12, Takeda discloses in figure 1, wherein the ESD sensing module comprises: a capacitor (7) having a first node and a second node, wherein the first node of the capacitor is operably coupled to a pin (2) of the integrated circuit that is susceptible to the ESD event; and a resistor (6) having a first node and a second node, wherein the second node of the resistor is coupled to the first or second power pin(1) (V_{DD}) of the integrated circuit and the first node of the resistor is coupled to the second node of the capacitor to provide the corresponding sensed voltage. The Takeda reference at (col. 5, lines 53-65) discloses a time constant of the resistor and the capacitor is greater than a rise time of the ESD event, is less than a rise time of a power supply of the integrated circuit (V_{DD} rampup greater then RC time constant, and is independent of the given duration provided by the time latched module because the value of RC defines the time constant. As to claims 3 and 11, Takeda discloses in figure 1, wherein the ESD triggering circuit comprises: an ESD sensing module (8) operably coupled to sense the ESD event and provide a corresponding sensed voltage; and a timed latch module (3) operably coupled to provide, for a given duration, the clamping signal based on the corresponding sensed voltage (see col. 1, lines 54-65).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grassian 2004/0083315 in view of Mentzer 5535086.

As to claim 9, Grassian discloses in figure 1, An integrated circuit of use in a multiple function handheld device, wherein the integrated circuit comprises: a processing module (20) operably coupled to perform at least one algorithm (30) relating to a function of the multiple function handheld device (see page 1, [0011]); a multimedia module (24) operably coupled to produce rendered output data from data corresponding to the processing of the at least one algorithm by the processing module (see claim 1); at least one input pin operably coupled to the processing module; at least one output pin operably coupled to the multimedia module. However, Grassian does not explicitly disclose an electrostatic discharge (ESD) protection circuitry coupled to at least one of the input pin and the output pin, wherein the ESD protection circuitry includes: ESD clamping circuit operably coupled to a first power pin of the integrated circuit and a second power pin of the integrated circuit; ESD triggering circuit operably coupled to the ESD clamping circuit, wherein, when enabled and when sensing an ESD event, the ESD triggering circuit provides a clamping signal to the ESD clamping circuit such that the ESD clamping circuit provides a low impedance path between the first and second power pins; and ESD disabling circuit operably coupled to disable the ESD triggering circuit when the integrated circuit is in a normal operating mode. Takeda teaches the limitations as disclosed in the previously rejected claims. It would've been obvious to

one of ordinary skill in the and well known in the art at the time the invention was made to modify the device and add an electrostatic discharge protection circuitry in order to protect the equipment and sensitive data from being destroyed.

Allowable Subject Matter

Claims 5-8 and 13-16 are objected to as being dependent on a rejected base claim but would be allowable if written in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

For claims 5 and 13 and 13-16, the prior art of record does not disclose or suggest in the claimed combination: a timed latch module comprising a first and second nand gate wherein the first input of the first NAND gate is coupled to receive the corresponding sensed voltage; the second nand gate providing the clamping signal that is operably coupled to the second input of the first NAND gate; an inverter operably coupled to invert the corresponding sensed voltage to produce an inverted corresponding sensed voltage and a duration controlled delay module operably coupled to produce a pulse representation of the output of the first NAND gate.

For claims 6 and 14, the prior art of record does not disclose or suggest in the claimed combination: a first diode and second diode wherein the first diode is coupled from the input pin or the output pin to the first power pin; and a second diode coupled from the input pin or the output pin to the second power pin.

For claims 7 and 15, the prior art of record does not disclose or suggest in the claimed combination: a plurality of diode pairs operably coupled to a plurality of input pins and output pins, wherein the ESD triggering circuit is operably coupled to the plurality of diode pairs.

For claims 8 and 16, the prior art of record does not disclose or suggest in the claimed combination: the ESD disabling circuit comprising of an N-channel transistor coupled to the ground of the integrated circuit, wherein the drain of the N-channel transistor is coupled to disable the ESD protection circuit when it is biased on; and the delay module that enables the N-channel transistor after a delayed sensing of an ESD disabling signal.

The art of record does not disclose or suggest the above claimed features, nor would it be obvious to modify the art of record so as to include either of the above limitations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert T. Dang whose telephone number is 571-272-8326. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RTD

KARL D. EASTHOM
PRIMARY EXAMINER